INFORMATIONSTECHNIK UND ARMEE

Vorlesungen an der Eidgenössischen Technischen Hochschule in Zürich
im Wintersemester 1998/1999
Leitung:
Untergruppe Führungsunterstützung - Generalstab
Divisionär E. Ebert, Unterstabschef Führungsunterstützung

Mikrosensoren

Referent: Prof. Dr. H. Baltes

Mikrosensoren

Prof. Dr. H. Baltes

Inhalt

Micromachined Thermally Based CMOS Microsensors

Adresse des Autors:

ETH Hönggerberg HPT - H6
Labor für physikalische Elektronik
8093 Zürich

Informationstechnik und Armee
38. Folge 1998/99

also published in Proceedings of the IEEE, vol. 86, 1998, pp.1660-1678

05.99 30 8343/4

Published in *Proceedings of the IEEE*, vol. 86, 1998, pp. 1660-1678

Micromachined Thermally Based CMOS Microsensors

HENRY BALTES, MEMBER, IEEE, OLIVER PAUL, MEMBER, IEEE, and OLIVER BRAND, MEMBER, IEEE

Invited Paper

An integrated circuit (IC) approach to thermal microsensors is presented. The focus is on thermal sensors with on-chip bias and signal conditioning circuits made by industrial complementary metal-oxide-semiconductor (CMOS) IC technology in combination with post-CMOS micromachining or deposition techniques. CMOS materials and physical effects pertinent to thermal sensors are summarized together with basic structures used for microheaters, thermistors, thermocouples, thermal isolation, and heat sinks. As examples of sensors using temperature measurement we present micromachined CMOS radiation sensors and thermal converters. Examples for sensors based on thermal actuation include thermal flow and pressure sensors, as well as thermally excited microresonators for position and chemical sensing. We also address sensors for the characterization of process-dependent thermal properties of CMOS materials, such as thermal conductivity, Seebeck coefficient, and heat capacity, whose knowledge is indispensable for thermal sensor design. Finally, two complete, packaged microsystems —a thermoelectric air flow sensor and a thermoelectric infrared intrusion detector— are reported as demonstrators.

Keywords— *CMOS microsensors, micromachining, thermal sensor, thermopile, infrared sensor, flow sensor, pressure sensor, thermal converter, position sensor, chemical sensor, thermal conductivity, Seebeck coefficient, heat capacity.*

I. INTRODUCTION

Thermal sensors are sometimes considered a nuisance, since all sensors incidentally include undesirable, built-in temperature sensors, which produce cross-sensitivities described by temperature coefficients (TC's). In this paper, however, we dwell on the virtues of thermal sensors. They can be used as direct sensors to convert thermal measurands like temperature or heat to electrical signals. They can serve as indirect or tandem transducers to convert, e.g., radiation, electrical power, or the presence of chemical species through a temperature modulation to a final electrical output signal. Other kinds of indirect thermal sensors are based on thermal actuation effects such as resistive heating and thermomechanical effects (thermal expansion, bimorph effect). These can be exploited for thermal flow or pressure sensors and position or chemical sensors, respectively.

Thermal microsensors based on complementary metal-oxide-semiconductor (CMOS) technology became feasible when CMOS-compatible micromachining was established. Micromachining makes it possible to remove thermally conducting material (in particular the highly conducting bulk silicon) for thermal isolation of heated microstructures; this isolation is crucial for all thermal microsensors. While thermal effects are intuitively considered to be slow, the small size of CMOS microsensors brings about time constants in the ms and µs range. The merging of CMOS integrated cicuit (IC) technology and micromachining allows on-chip circuits; they are crucial to pick up small signals, e.g., the thermoelectric voltage in the µV range of CMOS infrared (IR) intrusion detectors [1]. The small size and low power consumption of CMOS microsensors allows battery-operated, pocket-size instruments, e.g., a complete air anemometer (flow velocity meter) of the size of a ballpoint pen [2].

Post-CMOS micromachining processes, first developed in university laboratories, include wet and dry etching for bulk and surface-micromachining. Wet etching can be applied from the front or the back of the finished CMOS wafer. Two of these processes have recently been transferred to European CMOS ASIC manufacturers interested in CMOS sensor production. One of these processes makes it possible to produce dielectric membranes with sandwiched polysilicon and metal structures for, e.g., thermopiles [3]. The other process produces, e.g., thermally excited silicon membranes for ultrasound transducers (up to 100 kHz) for proximity sensors [4, 5].

The paper is organized as follows: we begin, in Section II, with a summary of post-CMOS techniques, notably micro-

H. Baltes and O. Brand are with the Physical Electronics Laboratory, ETH Zurich, CH-8093 Zurich, Switzerland.

O. Paul is with the Institute of Microsystem Technology, University of Freiburg, D-79110 Freiburg, Germany.

This work was supported by the Swiss Priority Program MINAST.

machining, followed in Section III by a discussion of CMOS materials, physical effects, and CMOS structures pertinent to thermal sensors. Section IV is dedicated to sensors based on the detection of temperature modulation, while sensors using thermal actuation are the topic of Section V. Next, in Section VI, we present sensors for the characterization of thermal properties of CMOS materials. Two fully packaged thermal sensor microsystems are reported in Section VII. This paper complements and updates previous comprehensive papers [6, 7, 8, 9]. The goal of this paper is to illustrate the opportunities of CMOS thermal sensors by selected examples; completeness is not attempted.

II. Technology Summary

The fabrication technologies applied for silicon microsensors use materials and processes borrowed from the integrated circuit (IC) technology; the three main processes used in silicon microsensor fabrication are deposition, lithography and etching. These standard process steps allow batch-fabrication of microsensors similar to the fabrication of integrated circuits. Standard IC process steps are combined with special micromachining or deposition steps.

This paper focuses on the use of CMOS IC processes for the fabrication of thermally-based microsensors. The application of industrial CMOS processes limits the variety of materials and layer thicknesses available for transducer design. However, the transducer designer can benefit from the vast experience gained in the area of IC fabrication technology over the last decades. Moreover, the use of industrial CMOS processes enables the cointegration of mechanical microstructures for sensor and actuator applications with integrated circuits on the same chip.

Silicon sensors for temperature, optical radiation (e.g., charge coupled devices) and magnetic measurands (e.g., Hall plates and magnetotransistors) can be fabricated by industrial CMOS IC technology without further processing. Many other microsensors —including a variety of thermally-based microsensors— can be made by combining industrial CMOS technology with additional compatible processing steps, e.g., anisotropic etching of silicon or thin film deposition of "non-IC" materials. Preferably, the additional steps are performed as *post-processing* or *post-CMOS*, i.e., after completion of the regular IC process sequence. However, they can also precede the IC process (*pre-CMOS*) or can be performed in-between the regular IC steps (*intermediate processing*).

In the case of *post-processing*, the additional process steps have to be compatible with the foregoing IC process. To this end, the maximal process temperature is limited to about 400 °C in order to preserve the aluminum structures of the preceding IC process. Nevertheless, many standard micromachining steps, such as anisotropic etching of silicon or sacrificial layer techniques have been demonstrated to be compatible with industrial IC processes. In the following, post-processing micromachining steps commonly used for the fabrication of thermally-based microsensors will be briefly discussed.

Micromachined silicon microsensors is usually divided in two major categories by their fabrication technology: *bulk-micromachined* sensors which are fabricated by machining of the relatively thick silicon substrate and *surface-micromachined* sensors which are constructed from stacked thin films. Obviously, bulk-micromachining and surface-micromachining techniques can be combined. In the case of thermal microsensors, micromachining is usually employed to thermally isolate the sensor structure or part of it from the bulk silicon. This can be done by bulk-micromachining either from the front or the back of the wafer as well as by surface-micromachining steps. Fig. 1 illustrates six possible post-CMOS etching techniques.

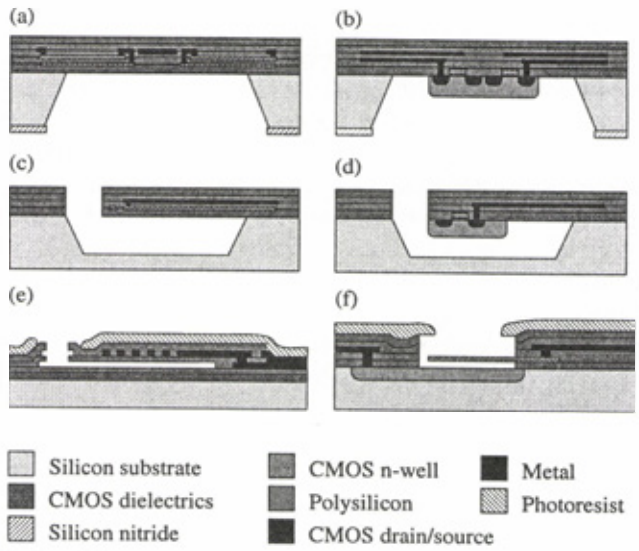

Fig. 1. Schematics of six post-CMOS micromachining techniques: rear bulk-micromachining (a) without and (b) with electrochemical etch stop on CMOS n-well; front bulk-micromachining (c) without and (d) with electrochemical etch stop; surface-micromachining based on (e) sacrificial aluminum and (f) sacrificial silicon oxide etching.

Membrane type structures can be released by anisotropic etching from the back of the wafer (see Figs. 1(a) and (b)). We refer to these process steps as *rear bulk-micromachining* in the following. The anisotropic etching step from the rear of the wafer is usually performed in a potassium hydroxide (KOH) solution [1, 10]. The etching characteristics of the different anisotropic etching solution for silicon are summarized, e.g., in [11, 12]. During the etching step the wafer front is usually protected from the etching solution by a mechanical housing. An additional dielectric or polymer layer on top of the CMOS passivation can be used to prevent accidental KOH break-through and, therefore, to increase the reliability of the micromachining process [3, 13]. The rear side of the fully processed wafers has to be prepared for the wet etching step. In order to ensure good etching results, a planar and defect free silicon surface must be achieved. The required surface quality can be obtained by chemical-mechanical polishing or using a spin etcher [3, 13]. A silicon nitride or silicon oxide layer is deposited and patterned on the wafer back to define the etch windows. A pro-

cess of this type has recently been transferred to the ASIC foundry *EM Microelectronic-Marin SA* (EM), Switzerland [1].

Membrane structures consisting of the dielectric layers provided by the CMOS process are obtained by etching through the complete silicon wafer (see Fig. 1(a)). The thermal oxide acts as etch stop. Dielectric membrane structures are used for sensors requiring excellent thermal isolation, such as the thermal radiation and flow sensors as well as the thermal converters discussed in this article. The stress within the thin dielectric membranes is crucial for the reliability of the mechanical structures. Typically, the thermal oxide is under compressive stress $\sigma = -300$ MPa [11]. The overall stress within the dielectric sandwich can be controlled by adjusting the intrinsic stress of the passivation layer.

Silicon membrane structures as well as complex suspended n-well structures are obtained by combining the anisotropic etching step with an electrochemical etch stop technique [10, 13]. The etching stops at the pn-junction between CMOS n-well and p-type substrate. During the electrochemical etching step, etching potentials have to be applied to the structural n-wells and the substrate. A special preparation sequence for the electrochemical etching of CMOS wafers is described in [13] and is available as foundry service by *Austria Mikro Systeme* (AMS), Unterpremstätten, Austria. The electrochemical etch-stop technique provides silicon-based microstructures which benefit from the excellent mechanical properties of silicon [14]. Moreover, active devices can be designed within the silicon structures. Depending on the wells available in the CMOS process used, only p-channel MOS devices [15] or unrestricted CMOS circuitry [10] can be embedded in the structural n-well.

As an example, Fig. 2 shows a photograph of a thermally isolated magnetotransistor microsystem [10]. The magnetotransistor is fabricated inside a suspended n-well in the center of the dielectric membrane. Heating resistors as well as temperature sensors allow temperature stabilization of the sensor. Therefore, offset variations due to ambient temperature variations are reduced [10]. The sensor has been fabricated using a 2 µm high-voltage CMOS process AMS. This process offers two n-wells with different diffusion depths in a p-type substrate. Each of the n-wells might contain a p-well and, therefore, unrestricted CMOS circuitry can be placed on the silicon microstructures. An additional reactive ion etching (RIE) step from the wafer front can be used to remove parts of the membrane structures and fabricate beams and bridges.

Cantilever beams, bridges and suspended membranes can also be released by *front bulk-micromachining*, i.e., an anisotropic etching step from the wafer front (Fig. 1(c) and (d)). Typically, the anisotropic etching is either performed in an ethylenediamine/pyrocatechol (EDP) or a tetramethylammonium hydroxide (TMAH) solution. Compared to KOH, these solutions usually offer lower silicon etch rates in <100> direction, but increased selectivity with respect to aluminum and silicon dioxide [12]. By overlapping an active area and contact, via, and pad openings in the sensor design,

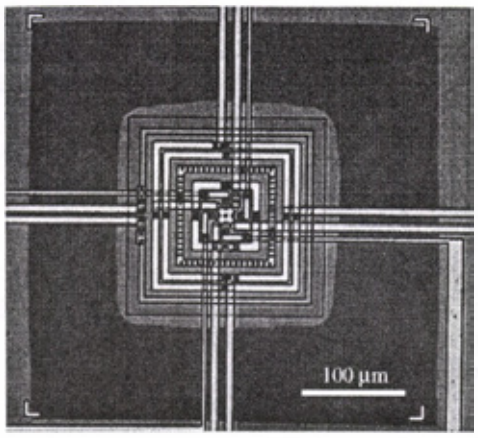

Fig. 2. Photograph of CMOS magnetotransistor in a suspended n-well; the sensor system is fabricated with a 2 µm high-voltage CMOS process of Austria Mikro Systeme and released by rear bulk-micromachining in combination with an electrochemical etch stop technique [10].

parts of the silicon substrate are directly exposed to the ambient and can be attacked by the etchant. Otherwise, the dielectric layers serve as a "natural" etch mask. Due to the anisotropic etching characteristics, convex corners in the design are underetched and microstructures, such as cantilever beams, can be released.

As an example, Fig. 3 shows a test structure [16] for measuring the heat capacitance of the thin film materials involved in the CMOS process (see Section VI). The struc-

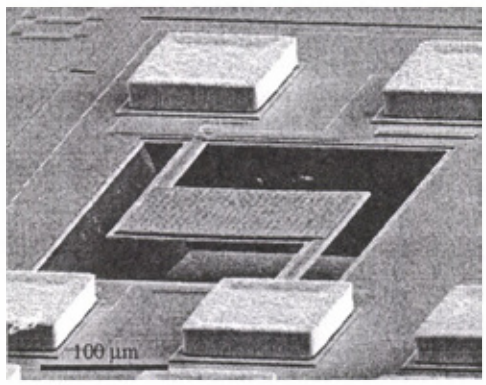

Fig. 3. SEM micrograph of microstructure to measure the heat capacitance of CMOS thin films; the device was released by a maskless front bulk-micromachining step using EDP [16].

ture consists of the dielectric layers of the CMOS process. Sandwiched in-between these layers are a polysilicon heating resistor as well as a metal layer.

The metal pads shown in Fig. 3 are covered with gold bumps. These gold bumps are electroplated on the metal pads of the CMOS processes of EM to prepare the CMOS dice for tape-automated-bonding. In a thermal sensor, the gold bumps can be used as a thermal mass to, e.g., increase thermal time constants [3] and reduce thermal cross-talk (see Section IV).

Similar to rear bulk-micromachining the anisotropic etching step from the front of the wafer can be combined with an electrochemical etch stop technique to release silicon micro-

structures (see Fig. 1(d)). Based on this technology, thermally isolated circuits, thermal vacuum sensors, and thermal converters have been realized [15, 17].

During the last years, dry etching methods [18, 19] based on *Reactive Ion Etching* (RIE) systems have been developed for bulk-micromachining in addition to wet etching methods. Commercial high-density, low-pressure plasma systems offering processes for silicon trench etching achieve typical silicon etch rates of several µm/min and aspect ratios up to 30 [18]. Trenches can be etched through a complete silicon wafer making the fabrication of a new generation of high aspect ratio structures possible. One major advantage of the dry etching methods is the independence of the anisotropy on the crystal orientation. Moreover, the dry etching processes can be performed as pre-, intermediate-, or post-processing.

Surface-micromachining techniques generate mechanical structures from stacked thin films. The basic technology is the sacrificial layer technique in which a mechanical structure is released by removing a sacrificial layer underneath it (Fig. 1(e) and (f)). Common sacrificial layer materials used in CMOS sensors are silicon dioxide [20, 21] and aluminum [22]. Silicon dioxide sacrificial layer etching is widely used for the fabrication of polysilicon microstructures [20, 21]. Sacrificial aluminum etching (SALE) [22] has been applied, e.g., for the fabrication of the thermal pressure sensor shown in Fig. 4 [23]. The metal pads are protected with photoresist during the etching step. The etching process releases a circular membrane consisting of the inter-metal oxide and the passivation of the CMOS process. The second metal layer sandwiched in-between these dielectric layers forms a thermistor for the thermal pressure sensing (see Section V). Another example of a microsensor released by SALE is the resonant fluid density sensor reported in [24].

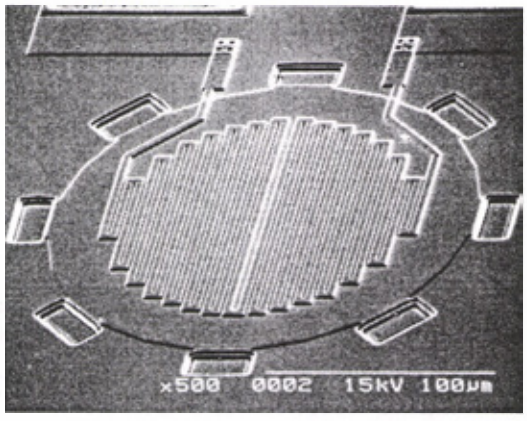

Fig. 4. SEM micrograph of thermal pressure sensor fabricated using industrial CMOS technology and released using post-CMOS sacrificial aluminum etching [23].

In addition to post-CMOS micromachining, thin-film materials can be deposited onto the sensor structures by a post-processing step. Examples are chemically sensitive layers, such as polymers, for chemical sensors [25] or soft-magnetic Ni-Fe films for improved sensitivity of magnetic sensor systems [26].

III. Basic Materials, Effects, and Components

Solid-state sensors require (i) physical or physicochemical transduction effects, (ii) materials exhibiting such effects, and (iii) structures isolating transduction effects from perturbations. For example, thermocouples use the Seebeck effect, materials with sufficiently large Seebeck coefficient, and thermally isolated and electrically connected legs.

Narrowed down to CMOS thermal microsensors, this means that we work under the following rules:

(i) use the materials provided by the CMOS IC process,

(ii) exploit the thermal (and coupling) effects inherent in the CMOS materials, and

(iii) design structures which bring out the transducer effects, but within the limits of the CMOS and post-CMOS fabrication rules (which are broader than the conventional CMOS IC design rules).

In this Section we summarize CMOS materials with respect to thermal properties and transduction effects and discuss basic transducer structures.

A. *CMOS Materials and Their Thermal Properties*

The CMOS materials include bulk silicon, polysilicon (possibly both n- and p-doped), dielectrics (silicon oxide, silicon nitride, passivation) and metal (alloy with mainly aluminum). In addition, epitaxial silicon is available in the case of BiCMOS technology. All these materials can serve as thermal mass. Silicon and metal conduct heat efficiently. The dielectric layers provide only moderate thermal isolation in view of their small thicknesses. That is why removal of material by micromachining is required for efficient thermal isolation.

Table 1 Measured material properties of a 1.2 µm CMOS process of AMS, a 2 µm CMOS process of EM, and a 1 µm CMOS process of ATMEL ES2; sheet resistance ρ_{sq}, temperature coefficient (TC) of ρ, majority carrier density *n(p)*, Seebeck coefficient α, and thermal conductivity κ, with error estimates [6].

	ρ_{sq} ±2 % [mΩ/cm]	TC of ρ [$10^{-3}K^{-1}$]	n(p) ±7 % [$10^{20}cm^{-3}$]	α ±5% [µV/K]	κ ±2.5 [W/(mK)]
AMS					
Gate-poly (n^+)	25	0.86	3.4	-120	28
Capacitor-poly (p^+)	215	-0.14	1.6	190	19
EM					
Gate-poly (n^+)	32	0.89	2.04	-108	19
Gate-poly (n)	2600	-4.40	0.04	-520	22
E2PROM-poly (n^+)	27	0.83	1.75	-111	17
Gate-poly (p^+)	425	0.59	0.33	330	20
ES2					
Gate-poly (n^+)	31	0.54	1.27	-108	16
Gate-poly (n^+)	45	0.49	0.93	-128	24

The thermoresistive effect (Joule heat) makes it possible to use the electrically conducting materials (notably polysilicon) for resistive heating, for example in integrated hot wire anemometers. The temperature coefficient of resistivity, notably that of polysilicon, is exploited for resistive thermometers (thermistors). The difference in thermopower (Seebeck coefficient) between different conducting CMOS materials (including differently doped silicon areas) is the basis of integrated thermocouples and thermopiles. The different thermal expansion coefficients of different CMOS materials produce the bimorph effect, which is exploited for the thermomechanical actuation of micromechanical structures.

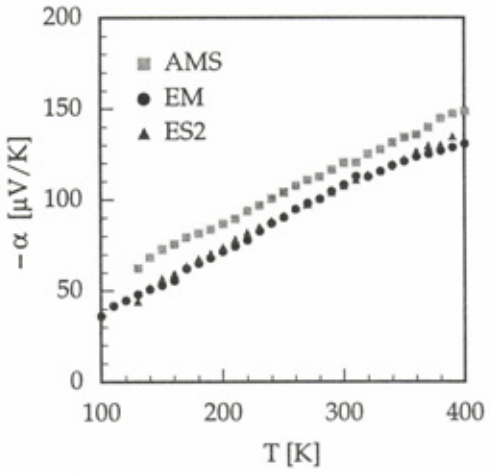

Fig. 5. Temperature dependent Seebeck coefficients of n^+-doped standard gate polysilicon layers of commercial ASIC CMOS IC foundries AMS, EM, and ATMEL-ES2.

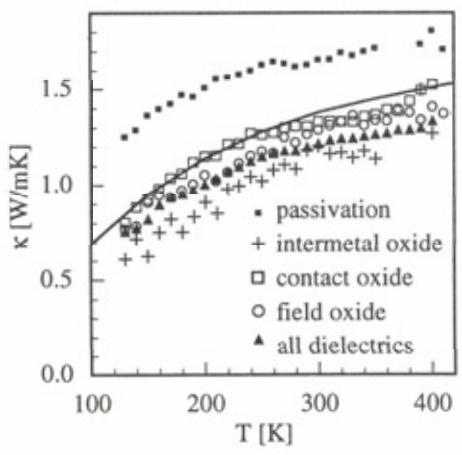

Fig. 6. Thermal conductivities of IC dielectric layers of a 1.2 μm CMOS process of AMS vs. temperature; recommended values for fused silica [27] are shown as solid line; uncertainties in κ are between 9 and 21 % [28].

The thermal properties of silicon depend on doping and structure (mono- or polycrystalline). For example, the temperature coefficient of the resistivity of polysilicon can be positive or negative, depending on doping. All material properties are temperature dependent. Moreover, the material properties are process-dependent and have to be known before an optimized thermal sensor can be designed for fabrication by a specific CMOS process.

Table 1 and Figs. 5 and 6 provide examples of such data. In Table 1, the temperature coefficients of resistivity, the Seebeck coefficients, and the thermal conductivities, of different polysilicon layers, from different CMOS IC processes and suppliers, are compared [6]. Figs. 5 and 6 show the temperature dependence of the Seebeck coefficient of polysilicon and the thermal conductivity of CMOS dielectric layers [28]. How to measure these and other material parameters is discussed in Section VI.

B. CMOS Resistors

CMOS resistors made of diffused silicon, deposited polysilicon, or metal lines can provide heating elements, thermistors, and strain gauges. The latter, while not being thermal devices in themselves, can be used to detect the thermal actuation of mechanical microstructures through the piezoresistive effect.

A meander-shaped metal line, sandwiched between two dielectric layers, several hundred microns long, a few microns wide, provides a heating resistor with a resistance of the order of 100 Ω. By exploiting its temperature coefficient of resistance of typically 3,000 ppm/K, the heating resistor can simultaneously act as thermistor for, e.g., temperature stabilization. Fig. 4 shows a photo of such a resistor used in a thermal pressure sensor [23].

Another option for monitoring heater temperatures is to locate a heating resistor and a thermistor side by side — as close as the design rules allow. An example is the polysilicon heater placed next to a polysilicon temperature measuring resistor, at the tip of a beam, as shown in Figs. 14 and 16(b).

Two adjacent meander-shaped polysilicon lines sandwiched in-between CMOS dielectrics can serve as an efficient pressure sensor [29]. Similarly, a single polysilicon filament provides a thermal radiation source [30]. Straight gate polysilicon heating resistors, several microns wide and several hundred microns long, are placed close to the hot contacts of a thermopile in thermoelectric gas flow sensors [2] and thermal converters [3], as shown in Fig. 7. Their resistance is typically 1 to 2 kΩ and their temperature coefficient is of the order of 800 ppm/K.

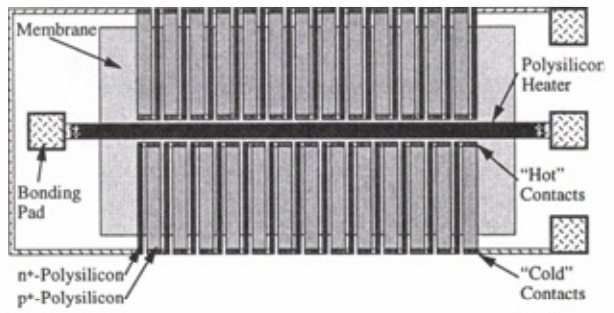

Fig. 7. Design layout of a CMOS thermal converter on a dielectric membrane: the unknown ac voltage is applied to the center polysilicon heater; an n^+/p^+ polysilicon themopile measures the resulting temperature increase [3].

C. CMOS Thermopiles

The CMOS metal, polysilicon, and diffused bulk silicon can serve as thermocouple material. Metal/polysilicon and n-polysilicon/p-polysilicon thermocouples can be sandwiched between the CMOS dielectric layers and thermally isolated by removal of the bulk silicon. Thermocouple performance is described in terms of the relative Seebeck coefficient α_{ab} between two materials (a) and (b) forming the thermocouple and the optimum figure of merit Z_{opt} defined by

$$Z_{\text{opt}} = \alpha_{ab}^2 [(\rho_a \kappa_a)^{1/2} + (\rho_b \kappa_b)^{1/2}]^{-2} \quad (1)$$

with electrical resistances ρ_a and ρ_b and thermal conductivities κ_a and κ_b of the two materials [3]. Table 2 shows these two parameters for the various combinations of CMOS metal and polysilicon for a specific process [3].

Table 2 Relative Seebeck coefficient α_{ab} (upper-right part) and figure of merit Z_{opt} (lower-left part) for polysilicon and metal combinations of the 2 µm CMOS technology of EM Marin [3].

α_{ab} [µV/K] Z_{opt} [1/K]	n^+-Poly1	n-Poly2	n^+-Poly2	p^+-Poly2	Metal1 Metal2
n^+-Poly1		410	3	441	109
n-Poly2	$6.4\ 10^{-6}$		413	851	519
n^+-Poly2	$1.1\ 10^{-8}$	$6.5\ 10^{-6}$		438	106
p^+-Poly2	$4.2\ 10^{-5}$	$1.8\ 10^{-5}$	$4.1\ 10^{-5}$		332
Metal1 Metal2	$4.2\ 10^{-5}$	$1.2\ 10^{-5}$	$3.9\ 10^{-5}$	$3.4\ 10^{-5}$	

Thermopowers are as high as several hundred µV/K, while the optimum figures of merit are low (compared to leading exotic ternary compounds) because of the higher resistivity of the polysilicon. The n^+-polysilicon/p^+-polysilicon combination is preferable [2, 3].

CMOS thermopiles typically consist of 5 to 100 thermocouples embedded in dielectric membranes with internal resistance of kΩ to MΩ and thermal conductance of the order of 0.1 mW/K. Thermopowers and sensitivities up to about 10 mV/K and 100 V/W, respectively, are achievable. A typical design is shown in Fig. 7. Applications are presented in Sections IV and V.

D. Thermal Isolation and Heat Sink Structures

Thermal isolation of the microsensors from all sources or sinks of heat other than those pertaining to the measurand are required. Low thermal mass is crucial for sensitivity. Thermal isolation is strongly improved by removing bulk silicon and embedding thermal microsensors in dielectric cantilever beams, bridges, or membranes. Polysilicon or (worse) metal lines remain as vehicles of heat transfer, as well as the surrounding air.

On the other hand, high thermal conductance is required for heat sinks and thermal uniformization. This can be provided by metal, bulk silicon, and polysilicon. The silicon substrate usually serves as the keeper of the ambient reference temperature for, e. g., the cold contacts of thermopiles. An example of uniform temperature achieved by a metal layer is shown in Fig. 14. Thanks to the metal layer above the heater and the thermistor, temperature uniformity is improved from several degrees to a fraction of one degree.

IV. Sensors Using Temperature Measurement

A. Thermal Radiation Sensors

Uncooled thermal infrared (IR) detectors have applications in building control, motion and presence detection, radiation thermometry, and night vision. In thermal IR sensors, incoming IR radiation is absorbed and converted into heat, and the resulting temperature increase ΔT is converted into an electrical output signal. In CMOS-based IR detectors, conversion is performed with integrated polysilicon/metal or bidoped polysilicon thermopiles (thermoelectric IR detectors) or with integrated thermistors (IR bolometers). A prerequisite for maximum responsivity is the efficient thermal isolation of the absorber. Surface-micromachined plate structures [31,32] and bulk-micromachined bridges [33,34] or membranes [35,36,37] composed of thin film dielectrics have provided appropriate supporting structures.

Besides single- and two-pixel CMOS IR detectors with [37,38,39] and without [33,34] on-chip circuitry, recent efforts have focussed on integrated IR detector array microsystems. IR microbolometer arrays produced by Honeywell [31] are based on surface-micromachined absorbers with integrated polysilicon resistors elaborated on top of a silicon substrate with peripheral multiplexers and transistors underneath each bolometer. The 50 µm by 50 µm wide pixels have a noise equivalent (NE) temperature difference of 0.039 K. Similar devices with VO_2 resistor achieve a NE power density of 0.04 nW/√Hz [32].

Two types of thermoelectric 1024-pixel arrays fabricated using a custom 3 µm single-metal single-poly p-well CMOS process with modifications at the front and back ends of the process have been reported recently [40]. The single polysilicon layer can be either n- or p-doped. Bidoped polysilicon thermopiles are integrated into rear-etched membranes and front-undercut suspended plates made of stress-compensated oxide-nitride dielectrics. The roughly 300 µm by 300 µm large pixels have respective responsivities of 12 V/W and 15 V/W, with time constants below 5 ms.

Fully CMOS compatible thermoelectric infrared arrays have been fabricated using the commercial 1 µm single-poly double-metal CMOS process of EM. Membranes composed of the standard CMOS dielectrics with stress-compensating passivation contain the two-dimensional arrays of IR pixels, with a pitch of 330 µm. Polysilicon/aluminum thermopiles are sandwiched between the dielectrics. The fabrication relies on the rear bulk-micromachining technique described in Section II. Thermal isolation of the pixels and mechanical stabilization of the membrane are achieved by gold lines

with a height and width of 25 µm, electroplated onto the CMOS dice using the standard bumping process of EM [1]. This allows the industrial fabrication of membranes with sizes up 14 mm by 16 mm. The pixels have responsivities of 4.1 V/W and time constants below 10 ms. Pixel-to-pixel cross-talk is below 2000 ppm.

A multiplexer and amplifier system consisting of an input and output modulator, a fully differential chopper preamplifier, a bandpass filter, and a third gain stage are cointegrated with the arrays. The preamplifier achieves an exceptionally low noise power density of 15 nV/√Hz, 1.5 µV offset, and a CMRR (common mode rejection ratio) of 70 dB [41]. The thermopile resistance of 2 kΩ is matched to the amplifier characteristics. The component characteristics make it possible to achieve an overall NE power of the detector/amplifier system of 39 nW per pixel for a bandwidth of 100 Hz. No vacuum package is required for this performance. An example of a CMOS IR detector array microsystem is shown in Fig. 8.

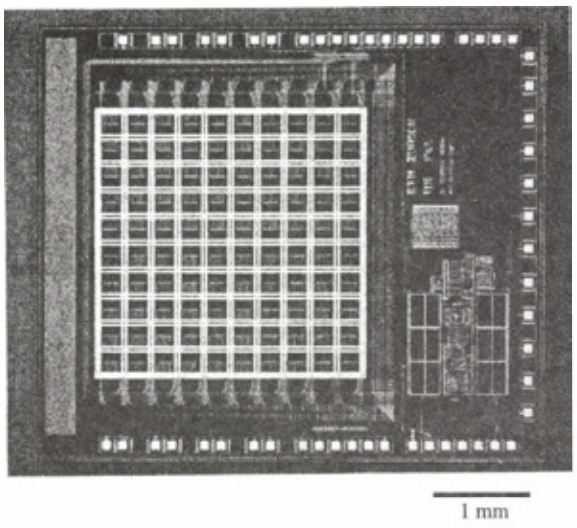

Fig. 8. Photograph of rear bulk-micromachined CMOS IR detector array microsystem with on-chip amplifier system fabricated using a 1 µm CMOS process of EM; 10 by 10 pixels are located on a dielectric membrane stiffened by electroplated gold lines; overall chip dimensions are 6.3 mm by 5.4 mm [1].

B. Thermal Converters

Thermal converters cover a broad range of applications including true rms conversion, ac-dc standards, and power meters. In comparison with mechanical or analog circuit based converters, thermal devices offer improved bandwidth and higher crest factor capability. Integrated true rms thermal converters often contain two thermal elements, i.e., a sensor and a reference each containing a heater and a temperature monitor. An ac voltage V_{in} (or current I_{in}) to be measured is dissipated in one device, while the other is heated with a dc signal V_{dc} (or current I_{dc}). Using a feedback loop, the dc input is adjusted to the level where both devices experience identical temperature increases. Since two identical thermal elements are used side by side, non-linearities of the individual elements and temperature-dependent material properties are compensated.

An early micromachined CMOS thermal converter with on-chip circuitry was reported by Yoon et al. [42]. Its fabrication relied on a custom 3 µm CMOS process. Each thermal converter contains two polysilicon heating resistors and a Au/Cr thermistor on an oxide/nitride membrane. The system has an input dynamic range of 60 dB and achieves a – 3 dB bandwidth of 20 MHz [42].

Electrochemical front etching makes it possible to fabricate CMOS thermal converters using an unmodified CMOS process [43]. Single-crystalline silicon islands suspended on oxide beams contain a polysilicon heater and a temperature sensing diode. The system achieves a sensitivity of 74 V/W, a dynamic range of 53 dB, and a -3 dB bandwidth of 415 MHz. Linearity is better than 1 % below 1 mW input power [43].

Thermoelectric CMOS thermal converters were pioneered by Jaeggi et al. [3,44,45] and Gaitan et al. [46]. Recent prototypes are based on dielectric membranes fabricated using the rear bulk-micromachining technique described in Section II. A device on a 560 µm by 1060 µm large membrane composed of the CMOS dielectrics contains a 1000 Ω gate polysilicon heating resistor and 66 n^+-polysilicon/p^+-polysilicon thermocouples with a total resistance of about 720 kΩ [3]. The sensitivity of the device is 129.6 V/W with a TC of -278 ppm/K. Its nonlinearity is 1% at an input of 2 V. It has a thermal time constant of 10.5 ms and achieves a -3 dB bandwidth of 700 MHz.

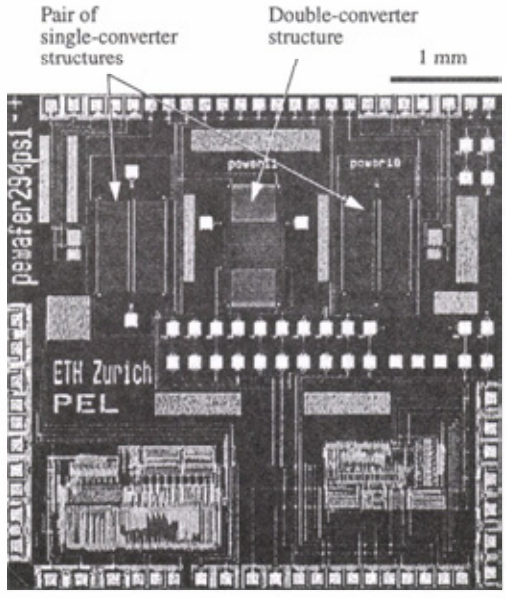

Fig. 9. Microphotograph of CMOS thermal converter chip including a pair of thermal converters on two membranes (top left and right), a double-converter structure on a single membrane (top center), the interface circuit and the incremental A/D converter [3, 49].

Two such devices were combined on a chip with an on-chip low-noise transconductance amplifier and incremental A/D converter, see Fig. 9 [3,47,48,49]. The amplifier has a transconductance of 637 µS, output resistance of 12.2 MΩ, gain of 77 dB, and input-referred offset of 1 µV. At a clock frequency of 50 kHz and with a reference voltage $V_{ref} = \pm 0.5$ V, the A/D converter achieves a resolution and

linearity of 12 and 10 bits, respectively. The system provides an oversampled digital output, the mean value of which is proportional to V_{in}^2/V_{ref}^2. Up to an input voltage of 2 V, the overall system nonlinearity is smaller than 0.1%.

A double-converter structure unites sensor and reference, each consisting of a heater and a thermopile, on a single membrane. The device (see Fig. 9) requires half the area of the two-membrane system and achieves similar specifications [3,45]. Finally, a device with 50 Ω heater is optimized for high frequencies. It has a -3 dB bandwidth larger than 1 GHz [3].

V. Sensors Using Thermal Actuation

A. *Thermal Flow Sensors*

Thermal CMOS flow sensors measure the convective heat transport by a fluid. The measurement is usually performed by thermally isolated structures such as cantilevers [50, 51], bridges [52,53,54,55,56,57], or membranes [2,57,58,59,60, 61] containing a heater and one or two temperature sensors. Heaters made of Pt [58,61], an unspecified metal [53], or polysilicon [50,52,54,56,57,59,62,63] have been used. Temperatures are monitored by metal [53,58,61] or polysilicon [55,62] thermistors, polysilicon/metal [50,56,57,60], or n^+-polysilicon/p^+-polysilicon [2,59] thermopiles, or integrated diodes [51,63].

Convective cooling is measured by miniaturized versions of the classical hot wire anemometer [50,52,59]. In these structures the power P needed to maintain a temperature difference ΔT between heater and the incoming gas flow is described by [64,65]

$$P = (c_1 + c_2\sqrt{v})\Delta T \ , \qquad (2)$$

where v denotes the flow velocity and c_1 and c_2 involve thermal properties of the microsensor and fluid.

A second class of devices exploits flow-induced thermal asymmetries. At a fixed heating power P, a velocity-dependent temperature difference $\Delta T(v)$ is measured between downstream and upstream locations on a centrally heated structure [2,53,56,57,61]. At small flow velocities, the response of such transducers is linear and does not show the square root behavior (Eq. 2) of hot wire anemometers.

Recent CMOS microbridge and membrane devices [56, 57] fabricated using IC technologies of EM and ATMEL ES2 exploit this principle. They contain standard gate polysilicon heating resistors (between 1.6 and 3 kΩ), and CMOS thermopiles. Depending on design parameters such as thermopile length and distance between heater and hot thermopile contact, and on the packaging geometry (channelled or free flow), sensitivities up to 0.92 $VW^{-1}m^{-1}s$ have been achieved. Velocities between 0.05 and 2 m s^{-1} of air forced through narrow ducts have been determined [57]. Accessible free flow velocities range from 0.05 to 38 m s^{-1} [2]. The response of such thermal devices is, to first order, proportional to the velocity surface gradient [57].

A recent flow sensor microsystem [2] combining a membrane sensor with on-chip power management, and signal amplification and conversion circuitry, with rectangular electroplated gold frame and bumps for flip-chip mounting, is shown in Fig. 10. Its packaging is described in Section VII.

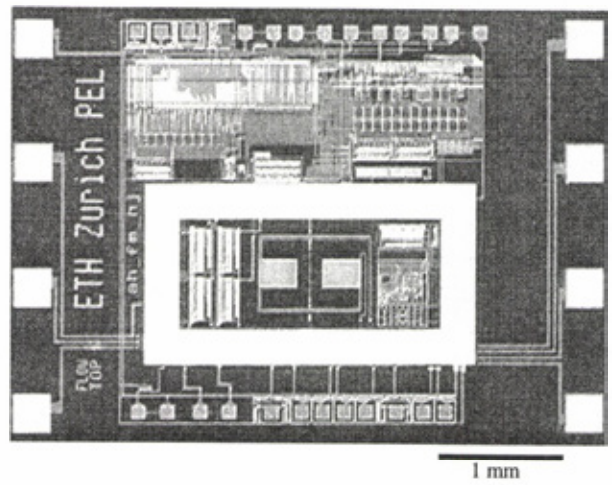

Fig. 10. Microphotograph of CMOS chip with integrated thermoelectric flow sensor and on-chip circuit including two amplifier stages, A/D converter, and power management. The rectangular frame and bumps consist of electroplated gold and are used for the flip-chip packaging of the device [2].

B. *Pressure Sensors*

Thermal pressure (p) microsensors are based on the pressure-dependent dissipation of either heat or momentum through a gas. So-called micro-Pirani gauges exploit the first principle and transfer thermal power from a heat source via the gas to a heat sink. Over a wide pressure range, such devices are characterized by a thermal conductance $G_{gas}(p)$ through the gas of the form

$$G_{gas}(p) = G_0 \cdot (1 + p_{1/2}/p)^{-1} \ , \qquad (3)$$

where the transition pressure $p_{1/2}$ is inversely proportional to the typical distance d between heat source and sink [66] and depends on gas and sensor surface properties. Thermally excited microresonators, on the other hand, transfer momentum and thus experience damping. This leads to a p-dependent contribution to the quality factor, i.e.,

$$Q_{gas}(p) = Q_0 \cdot (1 + p_{1/2}/p) \ , \qquad (4)$$

valid over a wide pressure range. Inclusion of the thermal conductance G_{mat} of sensor materials or intrinsic damping Q_{intr} of resonant structures lead to the overall thermal conductance $G(p) = G_{mat} + G_{gas}$ and the Q-factor $Q(p) = (Q_{intr}^{-1} + Q_{gas}^{-1})^{-1}$ [66].

Three pressure regions are commonly distinguished for both device types. In the *molecular* region, the inelastic mean free path λ of gas molecules is much larger than d. The device response then tends to G_{mat} or Q_{intr}. In the intermediate or *viscous slip* region around $p_{1/2}$, λ is comparable to d and the device sensitivity is maximal. In the viscous region finally, where $\lambda \ll d$, the device response saturates. The useful range of a thermal pressure sensor typically extends two orders in pressure above and below $p_{1/2}$ [66].

Conduction-based CMOS pressure sensors have been fab-

ricated using bulk- and surface-micromachining. Anisotropic front silicon etching has produced microbeams composed of CMOS dielectrics with integrated gate n^+-polysilicon resistor (of about 4.2 kΩ) [67]. The devices also contain an n^+-polysilicon/aluminum thermopile to monitor the temperature increase ΔT at a constant heating power or to control the temperature increase by adjusting the dissipated power. The devices have sizes of 150-250 µm by 155 µm. At 1 mW of power, temperature increases $\Delta T = 15$ K were obtained at ambient pressure. In vacuum, ΔT increased to 22 K, with $p_{1/2} \approx 0.7$ kPa. Front-etched CMOS polysilicon coils provide high heat transfer efficiency, with transition pressure $p_{1/2} \approx 10$ kPa [29].

Klaassen et al. demonstrated an electrochemically front bulk-micromachined pressure sensor. It consists of a heatable silicon island laterally supported by a dielectric beam. A useful range from 0.8 Pa to 9.2 kPa is reported [17].

surface-micromachined CMOS pressure sensors (see Fig. 4) have been produced using SALE, cf. Section II [23,68]. They consist of a circumferentially clamped plate made of the intermetal dielectric and passivation layers, suspended over the die and separated from the subjacent dielectrics by a 0.65 µm wide gap. A meander made of the second CMOS metal is integrated between the plate component layers. It is simultaneously used as heating element and thermistor. Structures with sizes between 100 and 400 µm and internal resistances between 10 and 100 Ω were fabricated. The devices have a $p_{1/2}$ of roughly 30 kPa. At base pressure the G value of, e.g., the 200 µm devices is 50 µW/K. At 10 bars, G increases to 600 µW/K [23].

Surface-micromachined pressure sensors have been cointegrated with power management and read-out interfaces. Building on a first microsystem prototype [69], four sensor structures are combined with four references, two A/D converters for current and voltage measurements, a differential amplifier and bandgap reference [70]. The system is shown in Fig. 11. It tracks the temperature increase ΔT of the sensors, adjusting it to roughly 6 K above the chip temperature. The thermal power necessary to maintain ΔT is measured and provided in digital form.

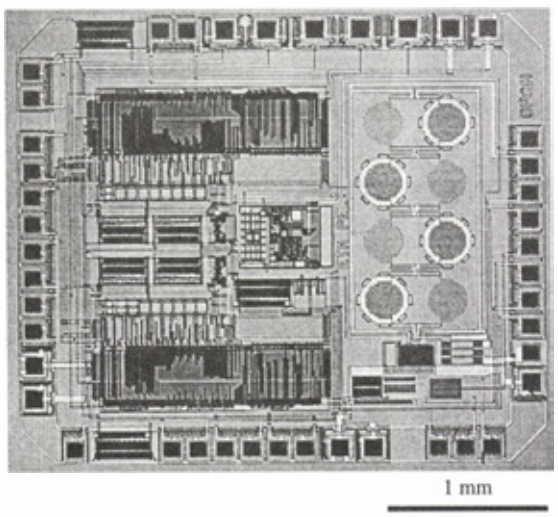

Fig. 11. Microphotograph of integrated pressure sensor microsystem consisting of pressure and reference sensors, front-end interface, bandgap reference, and two incremental A/D converters for current and voltage measurements [70].

Finally, resonant pressure sensors based on thermomechanically excited beams made of CMOS thin films, with sizes up to 200 µm by 300 µm have been demonstrated [67]. Two of their three suspension hinges contain integrated polysilicon heating elements, while two strain gauges are integrated into the center hinge. At 0.1 Pa and 10 kPa, the devices achieve $Q \approx 7000$-8000 and 200-300, respectively, with a transition pressure $p_{1/2} \approx 500$ Pa.

C. *Resonant Position Sensors*

Thermal actuation is a widely used driving mechanism for silicon based resonant structures [9,71] and often combined with piezoresistive detection of vibrations. The required polysilicon or monocrystalline silicon resistors are standard components of industrial IC processes.

As an example of a thermally excited resonant sensor, we briefly discuss the ultrasound barrier microsystem [5] shown in Fig. 12. It consists of an ultrasound transmitting and receiving element facing each other at distances up to 150 mm. The ultrasound transmitter is operated at its fundamental resonance frequency and continuously generates ultrasound which is detected by the receiver unless the object to be detected interrupts the sound path.

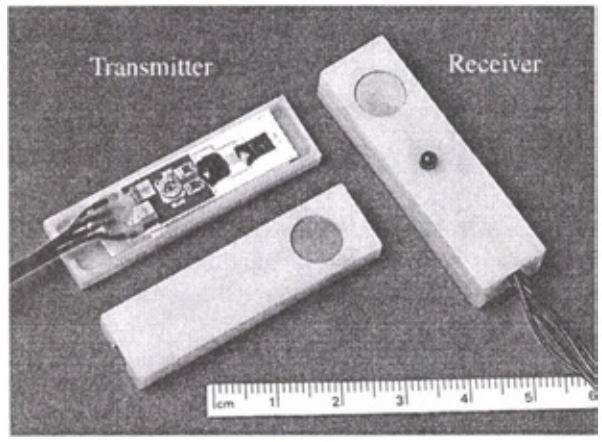

Fig. 12. Photograph of packaged, thermally actuated ultrasound barrier microsystem for object detection; the (open) transmitter consists of the membrane resonator, the ASIC with the driving circuitry, and a small number of passive SMDs mounted on a ceramic substrate; the ASIC as well as the bonding pads and bonding wires of the transducer chip are sealed with a commercially available epoxy; the top part of the microsystem package has an opening over the transducer element which is covered by a porous foil [5].

Micromachined membrane resonators are employed as ultrasound generating and receiving elements. The membranes are fabricated using post-processing anisotropic etching with electrochemical etch-stop. The resulting membranes consist of monocrystalline silicon covered with the dielectric layers provided by the silicon process. Diffused resistors in the membrane center and close to the membrane edges are used as excitation and detection elements, respectively. Transverse membrane vibrations are

generated by applying an ac voltage superimposed on a dc voltage to the driving resistor. With amplifying feedback-loop, the transmitting membrane is always operated at its fundamental resonance frequency of about 70-90 kHz. With an average heating power of 100 mW, typical vibration and sound pressure amplitudes of 300 to 400 nm and 0.25 Pa (at 50 mm distance), respectively, are obtained at resonance.

To obtain maximum output sensitivity of the system, the resonance frequency of the receiving element has to be tuned to that of the transmitter. This is achieved by applying a static thermal power to the receiving membrane, which shifts its resonance frequency [5].

Fig. 12 shows the packaged ultrasound barrier microsystem reported in [5, 72, 73]. The (open) transmitter element consists of the micromachined membrane resonator, an ASIC with the driving circuitry and a small number of passive, surface-mounted devices (SMD). Microsystem package and circuitry are described in detail in [72] and [74], respectively. A distance measurement system based on similar membrane resonators is presented in [73].

D. *Bimorph and Thermally Cycled Chemical Sensors*

Resonant silicon cantilever beams can be viewed as the silicon version of the quartz-crystal microbalance used, e.g., in deposition equipment to monitor film thicknesses. Assuming a small added mass compared to the mass of the resonator, the resonance frequency decreases linearly with the increasing mass. Due to the small mass of micromachined cantilever beams (typically of the order of 10^{-9} to 10^{-6} g), minimal detectable mass changes of the order of 10^{-12} g and below are feasible [75]. This makes silicon based resonators attractive for chemical sensing applications. To this end, a chemically sensitive layer is deposited onto the cantilever beam in an additional post-processing step. Polymer films such as polyurethane or polysiloxane derivatives are commonly used as chemically sensitive layers for monitoring hydrocarbons including halogenated compounds [76]. They offer a compromise between selectivity to specific analytes and reversibility of the polymer/analyte interaction. The polymer absorbs an amount of the analyte proportional to its concentration in the gas phase. The resulting mass change is monitored with the silicon microbalance. Additional heating resistors underneath the polymer layer can be used for desorption of the analyte.

As an example, Fig. 13 shows an SEM micrograph of a micromachined silicon cantilever beam. The beam resonator features electrothermal excitation and piezoresistive detection of transverse vibrations. The device was fabricated with a 2 µm CMOS process of AMS and released by a post-processing rear bulk-micromachining step with electrochemical etch stop on a CMOS n-well and a reactive-ion-etching step from the wafer front [25]. Finally, a layer of polyetherurethane was deposited on the beam.

Using a 300 µm by 300 µm silicon beam resonator with a fundamental resonance frequency of approximately 140 kHz and a Q-factor of 490 in air, the measured frequency shifts upon exposure to 4000 ppm ethanol and 2500 ppm n-octane are approximately 35 Hz and 70 Hz, respectively [77].

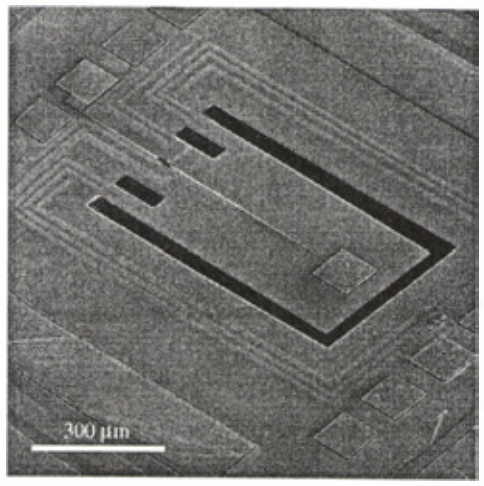

Fig. 13. SEM micrograph of a silicon cantilever beam resonator for chemical sensing; diffused resistors within the suspension beams allow electrothermal excitation and piezoresistive detection of vibrations [25].

VI. Sensors for Thermal Material Properties

Besides geometrical data such as layer thicknesses and lateral dimensions, reliable values of thermophysical material properties are essential for any meaningful simulation of thermal CMOS microsystems [78]. Properties of interest include (i) the temperature-dependent sheet resistance of CMOS conductors, (ii) the thermal conductivity κ of individual CMOS thin films, dielectrics and conductors, (iii) the thermopower α of semiconducting layers against metallization, and (iv) the heat capacity c of the layers.

Sheet resistances are routinely measured by the van-der-Pauw method [79]. Techniques to measure the other three classes of properties are described in the following subsections. They have in common the use of dedicated micromachined test structures optimized for the measurement of a single property. The devices are fabricated in standard CMOS technology followed by compatible front bulk-micromachining. Integrated in the process control modules of CMOS processes, they make it possible to assess the relevant process-dependent nonelectrical properties pertinent to thermal microtransducers. Reviews of results are given in [6,80,81,82,83]. Data are compiled in the database ICMAT [81].

A. *Thermal Conductivity*

Thermal microstructures like that shown in Fig. 14 make it possible to determine κ of CMOS thin films [28,84,85]. The structures are composed of a main cantilever with lateral arms, suspended over a front bulk-micromachined cavity. The cantilevers consist of various sandwiches of the CMOS layers, including dielectric films, polysilicon layers, and/or metallizations. By appropriate layout design, two gate polysilicon resistors are integrated into their free end.

One resistor is used as a heater, while the other serves as a thermistor. An integrated rectangular cover made of the CMOS metals homogenizes the temperature distribution over the two polysilicon structures. In view of the large surface-to-volume ratio of such thin film structures, precautions have to be taken to minimize radiative heat losses. This is achieved by shrinking the lateral dimensions of the structure to a few hundred micrometers [84].

When a power P is dissipated in the heater, the temperature of the cantilever tip is increased by ΔT. The ratio $P/\Delta T$ is equal to the thermal conductance G of the structure. $G = G_a + G_c$ is the sum of two contributions, namely the thermal conductances of the arms (index a) and the cantilever (index c), respectively. The latter contribution is given by

$$G_c = \sum \kappa_i d_i w_i / L , \qquad (5)$$

where the summation runs over the component layers of the cantilever and κ_i, d_i, w_i, and L denote their respective thermal conductivity, thickness, and relevant width and length. In order to determine κ_i of individual thin films, the composition of the cantilevers is systematically varied. The comparison of structures differing by a single layer allows the product κd of the layer to be extracted by subtracting one experimental G value from the other. For a double-poly, double-metal CMOS process with field oxide, contact oxide, intermetal dielectric, and passivation layer, a minimum of nine structures is required [28].

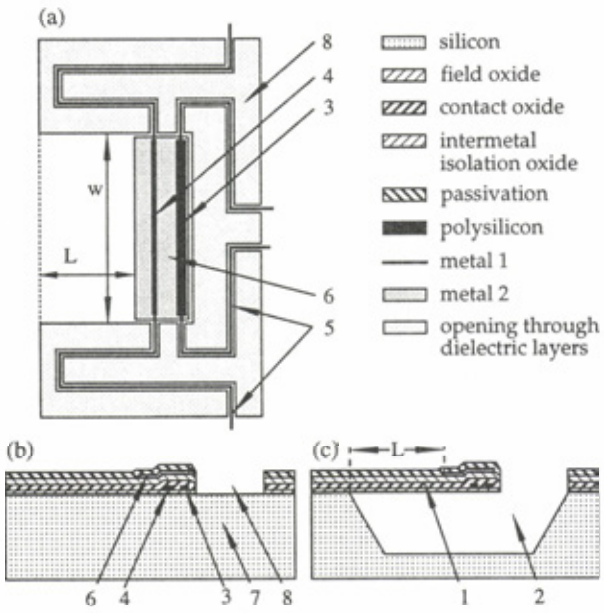

Fig. 14. Schematic top view (a) and cross-sections (b,c) of microstructure to determine thermal conductivities of CMOS thin film sandwiches; cross-sections are displayed (b) after CMOS process and (c) after post-processing. 1: cantilever, 2: etched cavity, 3: polysilicon heater, 4: polysilicon temperature monitor, 5; metal connections, 6: metal cover for temperature homogenization, 7: silicon substrate, 8: openings through CMOS dielectrics [28]; typical beam length L = 100 µm.

Using this method, it was found that thermally grown oxides have a κ between 1.08 and 1.28 $Wm^{-1}K^{-1}$. The κ of deposited thin oxide films varies between 0.91 and 1.65 $Wm^{-1}K^{-1}$. Between 120 and 420 K the temperature-dependent κ values of various silicon oxides generally lie within -35% and +15% [28,83] of the recommended value for fused bulk silica [27]. CMOS gate and capacitor polysilicon layers have thermal conductivities between 17.2 and 32.6 $Wm^{-1}K^{-1}$ at 300 K, with TC between -1100 and 0 ppm/K [28,82,83,84,85]. For comparison, κ of pure silicon is 156 $Wm^{-1}K^{-1}$ [27].

Aluminum-based CMOS metallizations investigated so far have shown thermal conductivities between 173 and 238 $Wm^{-1}K^{-1}$. These values are correlated with the electrical conductivity σ of the layers, and agree within 10% with the predictions of the Wiedemann-Franz law, $\kappa/\sigma = \pi^2 k_B^2 T/3q^2$, where k_B, T, and q denote Boltzmann's constant, absolute temperature, and elementary charge, respectively [82,83].

The above method provides in-plane thermal conductivities. A method to measure perpendicular thermal conductivities of CMOS thin films and interfacial thermal resistivities is described in [86]. The authors report κ values of between 1.0 and 1.14 $Wm^{-1}K^{-1}$ for PECVD silicon oxides.

B. Seebeck Coefficient

In view of its definition, the Seebeck coefficient of semiconductor materials can be measured using a thermocouple. A semiconductor sample is contacted at two ends; one end is heated, while the other is coupled to a heat sink. Contact temperatures T_1 and T_2 are monitored and the thermoelectric voltage V_{te} between the contacts is measured. For sufficiently small differences $\Delta T = T_2 - T_1$, the Seebeck coefficient $\alpha(T_{av}) = V_{te}/\Delta T$ is obtained at the average temperature $T_{av} = (T_1 + T_2)/2$. Early measurements for monocrystalline silicon and germanium were performed on macroscopic samples [87].

Single-crystal silicon samples with various p- and n-doping concentration against aluminum have been characterized using thermocouples diffused into silicon cantilevers [88]. The structures are produced by electrochemical and dry etching. Values of α between 0.3 and 0.5 mV/K at 300 K result for samples with doping concentrations used in practice.

The Seebeck coefficient of standard CMOS polysilicon layers against CMOS metal layers has been measured with polysilicon/aluminum thermocouples [80,82,89,90]. These are integrated into front bulk-micromachined cantilevers made of the full sandwich of dielectric CMOS layers. At their free end, the structures contain a heater and a thermistor for the measurement of temperature changes. Both are made of CMOS gate polysilicon. Heating powers of 125 µW establish temperature differences of roughly 10 K. As an example, for the n-doped gate and capacitor polysilicon layers of the double-poly double-metal 1.2 µm CMOS process of AMS, $\alpha = -107 \pm 1.5$ µV/K and $\alpha = -95.7 \pm 0.6$ µV/K, respectively, are found at 300 K.

A novel planar thermoelectric structure for the characterization of CMOS polysilicon has been reported recently [81, 90]. No micromachining is required for its fabrication. It is

ready for bonding and measurement after the CMOS process is completed. An optical micrograph and a schematic view are shown in Fig. 15. Its heart is a 670 µm long polysilicon strip with two contacts to the first CMOS metal. A 100 Ω polysilicon resistor close to one contact establishes the required inhomogeneous temperature over the sample. Thermocouple contact temperatures are monitored using thermistors made of the second CMOS metal. Temperature differences of 10 K are achieved with heating powers of 350 mW. In agreement with the results obtained using micromachined test structures, α values of -105.2±3 µV/K and -93.6±1.3 µV/K, respectively, were found for the two polysilicon layers of AMS' 1.2 µm CMOS process.

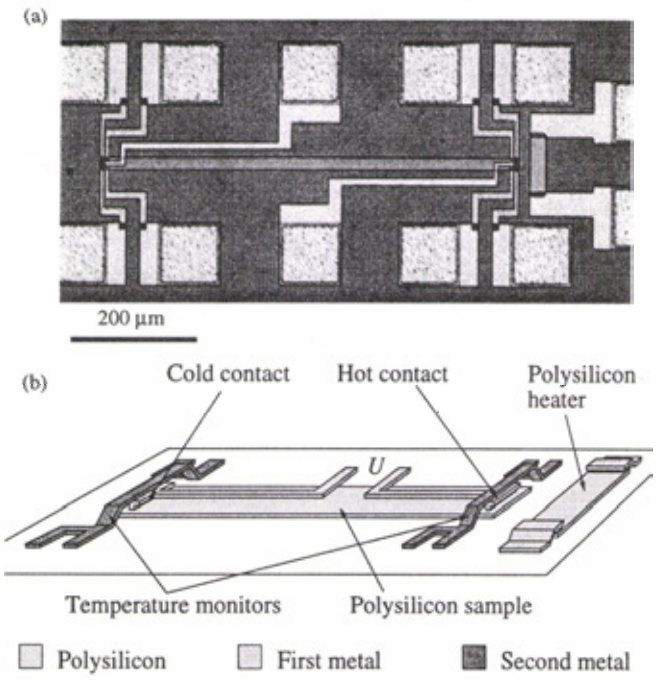

Fig. 15. (a) Optical micrograph and (b) schematic view of the planar test structure to determine the Seebeck coefficient of IC polysilicon layers. For clarity the dielectric layers and contact pads are not shown in (b) [90].

Generally, the thermopower of CMOS gate polysilicon (commercial ASIC processes) ranges between -89 and -120 µV/K. These layers are typically *n*-doped in the lower 10^{20} cm^{-3} range and have a TC of α of about 3×10^{-3} K^{-1} at 300 K [6,82,83].

C. *Heat Capacitance*

The individual heat capacities *c* of CMOS thin films affect the transient behavior of CMOS microtransducers. The determination of *c* requires accurate calorimetric measurements. Over the past years, four different microcalorimeters compatible with commercial CMOS processes have been reported [16,91,92,93]. They are schematically shown in Fig. 16. Each contains a polysilicon heating resistor. Heat dissipation by a current $I(t) = I_0 \cos(\omega t)$ establishes a time-dependent temperature profile with a component at the second harmonic angular frequency 2ω. The amplitude and phase of this component are monitored resistively or thermoelectrically.

The microbridge in Fig. 16(a) is composed of CMOS dielectrics and is heated with an integrated polysilicon resistor, which serves simultaneously as a temperature monitor [91]. Cantilevers such as those in Figs. 16(b) and (c) contain a polysilicon resistor near their free end [92,93]. Polysilicon thermistors (Fig. 16(b)) or polysilicon/aluminum thermocouples (Fig. 16(c)) are used for temperature measurements. Similar to the microbridge, the suspended plate structure in Fig. 16(d) contains a polysilicon heater/thermistor [16]. An SEM micrograph of this device is shown in Fig. 3.

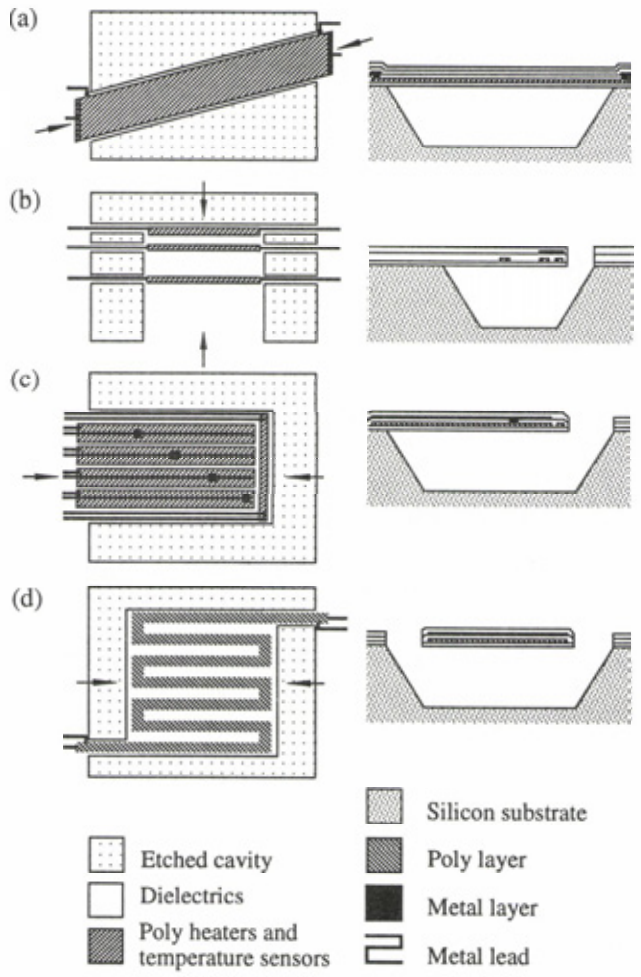

Fig. 16. Schematic top views and cross-sections of micromachined test structures used to determine the heat capacity of CMOS thin films and layer sandwiches: (a) microbridge with polysilicon heater/thermistor, (b) cantilever with polysilicon heaters and thermistors, (c) cantilever with polysilicon heater and integrated thermocouples, (d) suspended plate with polysilicon heater/thermistor; cross-sections are taken between the arrows.

In the cantilever structures, the ω-dependent propagation of the heat wave from the heater along the beam is quantified [92,93]. Temperature amplitude and phase depend on the average thermal diffusivity of the beam, *K*/*C*, with

$$K = \sum \kappa_i d_i w_i \,, \tag{6}$$

$$C = \sum c_i \rho_i d_i w_i \,. \tag{7}$$

Summations include all component layers of the cantilever with w_i, c_i, and ρ_i denoting the respective widths, heat capacities and densities of the component layers of the can-

tilever cross-section. The thermal diffusivity is experimentally determined. With a K value independently measured under static heating conditions, C of the main beam is then obtained. Using structures with different main beam compositions and measured cross-sectional areas, average volumetric heat capacities (VHC, in units of $J\,m^{-3}K^{-1}$) $\sum c_i \rho_i d_i w_i / \sum d_i w_i$ and $c_i \rho_i$ of individual layers are obtained. An average heat capacity of 1.66±0.06 MJ $m^{-3}K^{-1}$ was determined for a typical CMOS microtransducer sandwich composed of all dielectrics, polysilicon, and one metal layer [93]. A commercial CMOS passivation has a VHC of 1.82±0.12 MJ $m^{-3}K^{-1}$ [93]. The stack of CMOS dielectrics and a first CMOS metal layer have average VHC of 1.74±0.13 MJ $m^{-3}K^{-1}$ and 2.23±1.87 MJ $m^{-3}K^{-1}$ [92]. Recent measurements with plate structures have provided more accurate VHCs of CMOS metallizations between 2.45±0.21 MJ $m^{-3}K^{-1}$ and 2.81±0.34 MJ $m^{-3}K^{-1}$ [16].

VII. Packaged Thermal Sensor Demonstrators

While industrial manufacturing of micromachined CMOS sensor chips is taking off, their packaging needs a special development effort, case by case, before it may become routine. IC packaging techniques cannot be simply transferred to sensor packaging in view of the following [94]:

(i) In usual IC packages, the silicon die is sealed off from the environment, while at least part of the sensor die is exposed to the media sensed.

(ii) The sensor requires a die protection coating not required for sealed IC chips.

(iii) Sensor packaging is done before assembly, while the plastic molding of IC chips is done after die and wire bonding.

(iv) Sensors need elastic die attach material of sufficient thickness not required by IC chips.

(v) In contrast to IC wire bonding, sensor wire bonding has to be done at lower temperatures and while the chip sits on an elastic die attach.

Apart from such empirical rules, there is no generic sensor packaging technique. We therefore narrow down on two case studies: the packaging of micromachined thermoelectric CMOS air flow and infrared sensors.

A. *Packaged Thermoelectric Air Flow Sensor*

The microsystem die (see Section V, Fig. 10) is flip-chip mounted on a flexible substrate ("flex") fabricated by Dyconex, Zurich, Switzerland [2]. The flex is plugged into a standard socket, as shown in Fig. 17. An opening in the flex substrate is aligned with the sensor and enables free advection. For the flip-chip assembly, 25 µm high gold bumps and a gold frame surrounding the sensor are electroplated onto the chip using the standard bumping process of EM normally used for tape-automated bonding. The electrical interconnections between the chip bumps and the substrate contact pads are soldered with $PbIn_{50}$. In the same fabrication step, the bump frame is soldered to a corresponding

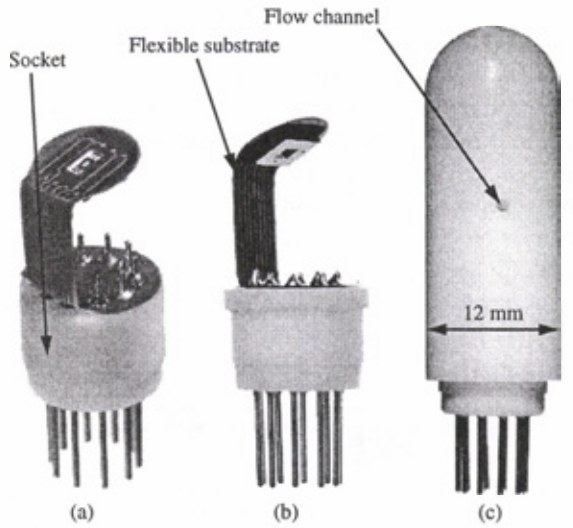

Fig. 17. Packaged micromachined flow sensor: chip/flex/socket unit (a, b) before and (c) after insertion into plastic housing [2].

structure on the substrate, thus sealing the electronics from the medium flowing over the sensor membrane. Finally an underfill is applied between chip and substrate.

The assembly is then inserted into a plastic housing consisting of a cylinder with a 1 mm wide flow channel. The sensor is tangent to the channel. The total volume of the anemometer is 2.8 cm^3. This progress in miniaturization (compared to currently available handheld air flow meters) is due to the unique combination of bulk-micromachining, industrial CMOS IC technology, and flip-chip technique. Fig. 18 shows the anemometer digital output signal for wind measurements up to 38 m/s. The dynamic range of the device is 65 dB. The system output is nonlinear and levels off at high wind speeds.

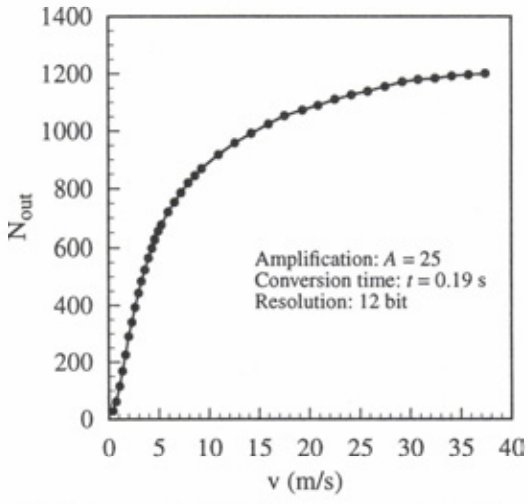

Fig. 18. Digital output signal N_{out} of the anemometer in upright position as a function of the air velocity v [2].

B. *Packaged Thermoelectric Infrared Sensor*

The following low-temperature packaging technique for integrated microsystems requiring hermetic packaging has

been demonstrated with the encapsulation of a micromachined CMOS infrared detector [95]. An infrared filter is directly attached to the sensor die using an on-chip gold spacer frame electroplated by the above standard bumping technology. Sensitive components such as the integrated circuit (picking up sub-μV signals) and the infrared pixels are hermetically sealed off and effectively screened from undesired environmental influences.

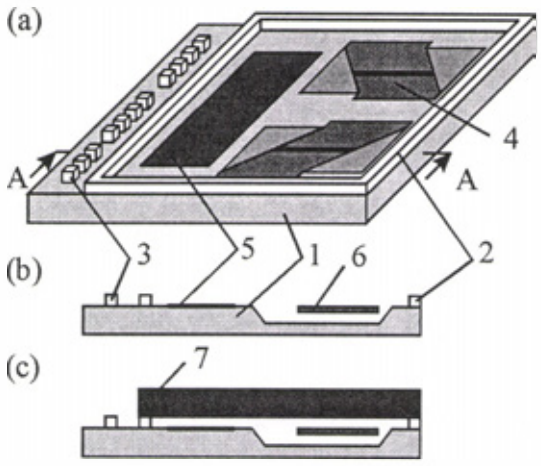

Fig. 19. Schematic view of the front bulk-micromachined infrared sensor: (a) schematic of the die; (b) cross-section A-A after bulk-micromachining, and (c) cross-section after final assembly; shown are (1) the sensor die, (2) the gold spacer frame, (3) the contact bumps, (4) the IR detector, (5) the circuitry, (6) the micromachined bridge, and (7) the wavelength filter [95].

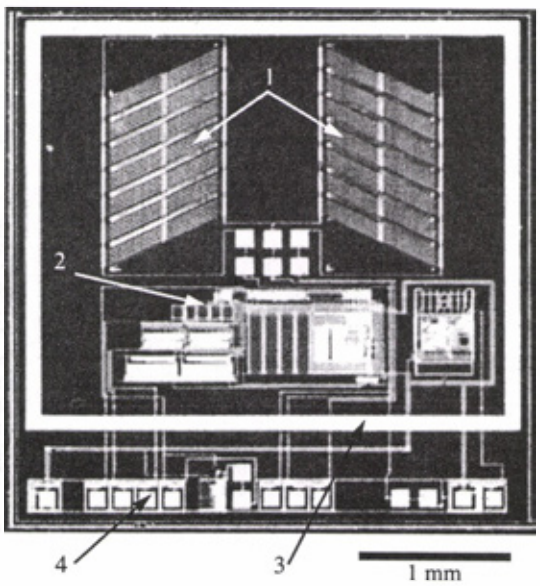

Fig. 20. Die of front bulk-micromachined infrared sensor microsystem; shown are (1) the IR detectors, (2) the read-out circuitry, (3) the gold spacer frame, and (4) the contact bumps [95].

The process is based on the diffusion bonding of a silicon filter onto the gold spacer using a sputtered aluminum layer. Annealing at 350°C for 33 minutes under a bonding pressure of 45 MPa produces bonds with a shear strength larger than 70 MPa. The bonding zone consists of a gold-aluminum (Au_4Al) intermetallic layer. Thermal aging at 155°C for 1000 h shows no changes in the interface metallurgy.

The sensor die shown in Figs. 19(a) and 20 contains two micromachined thermoelectric infrared detectors, each on a microbridge. Contact pads to the microsystem are located along one side of the chip. After completion of the CMOS process, gold structures are electroplated onto the silicon wafers using the bumping process. By appropriate design layout of the bumping mask, a rectangular gold frame surrounding the circuit and infrared pixels results, as is illustrated in Fig. 19(a) and 19(b).

The filter is a monocrystalline silicon plate coated with a stack of optical layers. The aluminum layer (thickness 1 μm) is sputtered onto the bonding area. The area above the circuit is also covered with aluminum to screen the circuit from radiation. The filter is then aligned and bonded to the gold frame as shown in Fig. 19(c).

VIII. Conclusion

We conclude that post-CMOS micromachining and deposition is viable for industrial production of thermal microsensors. CMOS-compatible tape automated bonding and flip-chip bonding can be drawn upon for hermetic sensor sealing. In the future, other ways of combining CMOS and micromachining may become practical for industrial microsensor fabrication. A likely candidate is pre-CMOS trench etching.

Acknowledgment

The authors are greatly indebted to current and former staff of the Physical Electronics Laboratory at ETH Zurich, notably Andreas Häberli, Mark Hornung, Dominik Jaeggi, Andreas Koll, Dirk Lange, Piero Malcovati, Felix Mayer, Thomas Müller, Ulrich Münch, Andri Schaufelbühl, Niklaus Schneeberger, Michael Schneider, Martin von Arx, and Marc Wälti, from whose publications they quote in this paper.

The excellent services of the prototype manufacturers Austria Mikro Systeme (Volker Kempe), ATMEL ES2 (Philippe Sagnol), and EM Microelectronic-Marin SA (Elko Doering) are gratefully acknowledged.

Financial support by the Swiss Priority Program MINAST is gratefully acknowledged.

References

[1] U. Münch, D. Jaeggi, K. Schneeberger, A. Schaufelbühl, O. Paul, H. Baltes, and J. Jasper, "Industrial fabrication technology for CMOS infrared sensor arrays," in *Digest Tech. Papers Transducers 97*, vol. 1, Chicago, 1997, pp. 205-208.

[2] F. Mayer, A. Häberli, G. Ofner, H. Jacobs, O. Paul, and H. Baltes, "Single-chip CMOS anemometer," in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1997*, Washington DC, 1997, pp. 895-898.

[3] D. Jaeggi, *Thermal Converters by CMOS Technology*, Ph.D. Thesis no. 11567, ETH Zurich, Switzerland, 1996.

[4] M. Hornung, O. Brand, O. Paul, and H. Baltes, "Ultrasound

transducer for distance measurements," in *Digest Tech. Papers Transducers 97*, vol. 1, Chicago, 1997, pp. 441-444.

[5] O. Brand, M. Hornung, H. Baltes, and C. Hafner, "Ultrasound barrier microsystem for object detection based on micromachined transducer elements," *J. Microelectromechanical Systems*, vol. 6, pp. 151- 160, 1997.

[6] H. Baltes, O. Paul, and D. Jaeggi, "Thermal CMOS sensors - and overview", in *Sensors Update,* vol. 1, Weinheim: VCH, 1996, pp. 121-142.

[7] P. Malcovati, H. Baltes, and F. Maloberti, "Progress in microsensor interfaces," in *Sensors Update*, vol. 1, Weinheim: VCH, 1996, pp. 143-171.

[8] H. Baltes, "Future of IC microtransducers," *Sens. Actuators A*, vol. 56, pp. 179-192, 1996.

[9] O. Brand, and H. Baltes, "Micromachined resonant sensors: an overview," *Sensors Update*, vol. 4, Weinheim: VCH-Wiley, 1998, in press.

[10] M. Schneider, T. Müller, A. Häberli, M. Hornung, and H. Baltes, "Integrated micromachined decoupled CMOS chip on chip," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 97*, Nagoya, 1997, pp. 512-517.

[11] A. Heuberger, *Mikromechanik*, New York: Springer, 1989.

[12] C. H. Mastrangelo and W. C. Tang, "Semiconductor sensor technologies," in *Semiconductor Sensors*, Ed. S. M. Sze, New York: Wiley, 1994, pp. 17-95.

[13] T. Müller, T. Feichtinger, G. Breitenbach, M. Brandl, O. Brand, and H. Baltes, "Industrial fabrication method for arbitrarily shaped silicon n-well micromechanical structures," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 98*, Heidelberg, 1998, pp. 240-245.

[14] K. E. Petersen, "Silicon as a mechanical material," *Proc. IEEE*, vol. 70, pp. 420-457, 1982.

[15] E. H. Klaassen, R. J. Reay, C. Storment, J. Audy, P. Henry, A. P. Brokaw, and G. T. A. Kovacs, "Micromachined thermally isolated circuits," in *Tech. Digest IEEE Solid State Sensor and Actuator Workshop,* Hilton Head, SC, 1996, pp. 127-131.

[16] L. Plattner, M. von Arx, O. Paul, and H. Baltes, "A floating plate structure to determine the heat capacity of CMOS thin films", *Sens. Materials*, 1998, in press.

[17] E. H. Klaassen, and G. T. A. Kovacs, "Integrated thermal conductivity vacuum sensor," in *Tech. Digest IEEE Solid State Sensor and Actuator Workshop,* Hilton Head, SC, 1996, pp. 249-252.

[18] E. H. Klaassen, K. Petersen, J. M. Noworolski, J. Logan, N. I. Maluf, J. Brown, C. Storment, W. McCulley, and G. T. A. Kovacs, "Silicon fusion bonding and deep reactive ion etching: a new technology for microstructures," *Sens. Actuators A*, vol. 52, pp. 132-139, 1996.

[19] G. T. A. Kovacs, and N. I. Maluf, "Bulk micromachining: wet and dry etching of deep microstructures," *Proc. IEEE*, this issue, pp. 1536-1551.

[20] R. T. Howe, B. E. Boser, and A. P. Pisano, "Polysilicon integrated microsystems: technologies and applications," *Sens. Actuators A*, vol. 56, pp. 167-178, 1996.

[21] J. Bustillo, R. T. Howe, and R. S. Muller, "Surface micromachining of integrated sensors and microactuators," *Proc. IEEE*, this issue, pp. 1552-1574.

[22] O. Paul, D. Westberg, M. Hornung, V. Ziebart, and H. Baltes, "Sacrificial aluminum etching for CMOS microstructures," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 97*, Nagoya, 1997, pp. 523-528.

[23] O. Paul, and H. Baltes, "Novel fully CMOS compatible vacuum sensor," *Sens. Actuators A*, vol. 46-47, pp. 428-431, 1995.

[24] D. Westberg, O. Paul, G. I. Andersson, and H. Baltes, "A CMOS-compatible device for fluid density measurements," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 97*, Nagoya, 1997, pp. 278-283.

[25] H. Baltes, D. Lange, and A. Koll, "IC microtransducers — new components with old materials?," in *Proc. SPIE*, vol. 3224, Austin, TX, 1997, pp. 2-13.

[26] M. Schneider, R. Castagnetti, M. G. Allen, and H. Baltes, "Integrated flux concentrator improves CMOS magnetotransistors," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 95*, Amsterdam, 1995, pp. 151-156.

[27] S. Touloukian, R. W. Powell, C. Y. Ho, and P. G. Klemens, *Thermophysical Properties of Matter*, vols. 1-2, New York: Plenum, 1970.

[28] O. Paul, M. von Arx, and H. Baltes, "CMOS IC layers: complete set of thermal conductivities", in *Semiconductor Characterization: Present and Future Needs*, Eds. W. M. Bullis, D. G. Seiler, A. C. Diebold, Woodbury, NY: AIP Press, 1995, pp. 197-201.

[29] N. Swart, and A. Nathan, "An integrated CMOS polysilicon coil-based micro-Pirani gauge with high heat transfer efficiency", in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1994*, San Francisco, 1994, pp. 135-138.

[30] M. Gaitan, M. Parameswaran, R. B. Johnson, and R. Chung, "Commercial CMOS foundry thermal display for dynamic scene simulation," in *Proc. SPIE*, vol. 1969, Austin, TX, 1993, pp. 363-369.

[31] R. A. Wood, "High-performance infrared thermal imaging with monolithic silicon focal planes operating at room temperature", in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1993*, Washington DC, pp. 175-178, 1993.

[32] H. Jerominek, M. Renaud, N. R. Swart, F. Picard, T. D. Pope, M. Levesque, M. Lehoux, G. Bilodeau, M. Pelletier, D. Audet, and P. Lambert, "Micromachined VO_2-based uncooled IR bolometric detector arrays with integrated CMOS readout electronics," in *Proc. SPIE*, vol. 2882, Austin, TX, 1996, pp. 111-121.

[33] R. Lenggenhager, H. Baltes, J. Peer, and M. Forster, "Thermoelectric infrared sensors by CMOS technology", *IEEE Trans. Electron Dev.*, vol. 13, pp. 454-456, 1992.

[34] R. Lenggenhager, and H. Baltes, "Improved thermoelectric infrared sensor using double poly CMOS technology", in *Digest Tech. Papers Transducers 93*, Yokohama, 1993, pp. 1008-1011.

[35] M. Müller, W. Budde, R. Gottfried-Gottfried, A. Hubel, R. Jahne, and H. Kück, "A thermoelectric infrared radiation sensor with monolithically integrated amplifier stage and temperature sensor", in *Digest Tech. Papers Transducers 95*, vol. 2, Stockholm, 1995, pp. 640-643.

[36] N. Schneeberger, O. Paul, and H. Baltes, "Optimization of CMOS infrared detector microsystems", in *Proc. SPIE*, vol. 2882, Austin, TX, 1996, pp. 122-131.

[37] R. Lenggenhager, D. Jaeggi, P. Macovati, H. Duran, H. Baltes, and E. Doering, "CMOS membrane infrared sensors and improved TMAHW etchant", in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1994*, San Francisco, 1994, pp. 531-534.

[38] P. Malcovati, C. Azeredo Leme, R. Lenggenhager, F. Maloberti, and H. Baltes, "Low-noise multirate SC readout circuitry for thermoelectric integrated infrared sensors", *IEEE*

Trans. Instrument. and Meas., vol. 44, pp. 795-798, 1995.

[39] C. Menolfi, Q. Huang, and N. Schneeberger, "A low noise thermoelectric infrared detector microsystem in a digital CMOS technology", in *Proc. ESSCIRC '96*, Neuchâtel, 1996, pp. 128-131.

[40] A. D. Oliver, W. G. Baer, and K. D. Wise, "A bulk-micromachined 1024-element uncooled infrared imager", in *Digest Tech. Papers Transducers 95*, vol. 2, Stockholm, 1995, pp. 636-639.

[41] C. Menolfi, and Q. Huang, "A low noise CMOS instrumentation amplifier for thermoelectric infrared detectors", *IEEE J. Solid State Circ.*, vol. 32, no. 7, pp. 1-9, 1997.

[42] E. Yoon, and K. D. Wise, "A wideband monolithic rms-dc converter using micromachined diaphragm structures", *IEEE Trans. Electron Dev.*, vol. 41, no. 9, pp. 1666-1668, 1994.

[43] E. H. Klaassen, R. J. Reay, and G. T. A. Kovacs, "Diode-based thermal rms converter with on-chip circuitry fabricated using standard CMOS technology", in *Digest Tech. Papers Transducers 95*, vol. 1, Stockholm, 1995, pp. 154-157.

[44] D. Jaeggi, C. Azeredo Leme, P. O'Leary, and H. Baltes, "Improved CMOS AC power sensor", in *Digest Tech. Papers Transducers 93*, Yokohama, 1993, pp. 462-465.

[45] D. Jaeggi, J. Funk, A. Häberli, and H. Baltes, "Overall system analysis of a CMOS thermal converter", in *Digest Tech. Papers Transducers 95*, vol. 2, Stockholm, 1995, pp. 112-115.

[46] M. Gaitan, J. Kinard, and D. X. Huang, "Performance of commercial CMOS-foundry-compatible multijunction thermal converters", in *Digest Tech. Papers Transducers 93*, Yokohama, 1993, pp. 1012-1015.

[47] P. Malcovati, A. Häberli, D. Jaeggi, F. Maloberti, and H. Baltes, "Oversampled A/D interface circuit for integrated ac-power sensor", in *Digest Tech. Papers Transducers 95*, vol. 1, Stockholm, 1995, pp. 119-122.

[48] A. Häberli, P. Malcovati, D. Jaeggi, H. Baltes, and F. Maloberti, "High dynamic range interface system for a micromachined integrated ac-power sensor", in *Proc. IEEE ISCAS 1995*, 1995, pp. 2241-2244.

[49] P. Malcovati, *CMOS Thermoelectric Sensor Interfaces*, Ph.D. Thesis no. 11424, ETH Zurich, Switzerland, 1996.

[50] D. Moser, R. Lenggenhager, and H. Baltes, "Silicon gas flow sensors using industrial CMOS and bipolar IC technology", *Sens. Actuators A*, vol. 25-27, pp. 577-581, 1991.

[51] G. Stemme, "An integrated gas flow sensor with pulse-width modulated output", in *Digest Tech. Papers Transducers 87*, 1987, pp. 364-367.

[52] D. Moser, R. Lenggenhager, G. Wachutka, and H. Baltes, "Fabrication and modeling of CMOS microbridge gas-flow sensors", *Sens. Actuators B*, vol. 6, pp. 165-169, 1992.

[53] R. G. Johnson, and R. E. Higashi, "A highly sensitive silicon chip microtransducer for air flow and differential pressure sensing applications", *Sens. Actuators*, vol. 11, pp. 63-72, 1987.

[54] Y. C. Tai, and R. S. Muller, "Lightly doped polysilicon bridge as an anemometer", in *Digest Tech. Papers Transducers 87*, 1987, pp. 360-363.

[55] T. Neda, K. Nakamura, and T. Takumi, "A polysilicon flow sensor for gas flowmeters", in *Digest Tech. Papers Transducers 95*, vol. 1, Stockholm, 1995, pp. 548-551.

[56] F. Mayer, O. Paul, and H. Baltes, "Influence of design geometry and packaging on the response of thermal CMOS flow sensors", in *Digest Tech. Papers Transducers 95*, vol. 1, Stockholm, 1995, pp. 528-531.

[57] F. Mayer, G. von Salis, O. Paul, and H. Baltes, "Scaling of thermal CMOS gas flow microsensors: experiment and simulation", in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 96*, San Diego, 1996, pp. 116-121.

[58] O. Tabata, "Fast-response silicon flow sensor with an on-chip fluid temperature sensing element", *IEEE Trans. Electron Dev.*, vol. 33, no. 3, pp. 361-365, 1986.

[59] D. Moser, and H. Baltes, "A high sensitivity CMOS gas flow sensor on a thin dielectric membrane", *Sens. Actuators A*, vol. 37-38, pp. 33-37, 1993.

[60] E. Yoon, and K. D. Wise, "An integrated mass flow sensor with on-chip CMOS interface circuitry", *IEEE Trans. Electron Dev.*, vol. 39, no. 6, pp. 1376-1386, 1992.

[61] M. Nagata, N. Swart, M. Stevens, and A. Nathan, "Thermal based micro flow sensor optimization using coupled electro-thermal numerical simulations", in *Digest Tech. Papers Transducers 95*, vol. 2, Stockholm, 1995, pp. 447-450.

[62] M. Parameswaran, A. M. Robinson, Lj. Ristic, K. Chau, and W. Allegretto, "A CMOS thermally isolated gas flow sensor", *Sens. Materials*, vol. 2, no. 1, pp. 17-26, 1990.

[63] R. Kersjes, and W. Mokwa, "A fast liquid flow sensor with thermal isolation by oxide filled trenches", *Sens. Actuators A*, vol. 46-47, pp. 373-379, 1995.

[64] L. V. King, "On the convection of heat from small cylinders in a stream of fluid", *Phil. Trans. R. Soc. A*, vol. 214, pp. 373-432, 1914.

[65] M. A. Lévèque, "Les lois de la transmission de chaleur par convection", *Ann. Mines*, vol. 13, pp. 201-239, 1928.

[66] O. Paul, O. Brand, R. Lenggenhager, and H. Baltes, "Vacuum gauging with complementary metal-oxide-semiconductor microsensors", *J. Vac. Sci. Technol. A*, vol. 13, no. 3, pp. 503-508, 1995.

[67] O. Brand, R. Lenggenhager, and H. Baltes, "Influence of air pressure on resonating and thermoelectric microstructures realized with standard IC technologies", in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1993*, Washington DC, 1993, pp. 195-198.

[68] O. Paul, and H. Baltes, "Thermal vacuum sensor by CMOS IC technology and sacrificial metal etching", *Sens. Materials*, vol. 6, no. 2, pp. 245-249, 1994.

[69] O. Paul, A. Häberli, P. Malcovati, and H. Baltes, "Novel integrated thermal pressure gauge and read-out circuit by CMOS IC technology", in *Tech. Digest IEEE Intl. Electron Devices Meeting IEDM 1994*, San Francisco, 1994, pp. 131-134.

[70] A. Häberli, O. Paul, P. Malcovati, M. Faccio, F. Maloberti, and H. Baltes, "CMOS integration of a thermal pressure sensor system", in *Proc. IEEE ISCAS 1996*, vol. 1, Atlanta, 1996, pp. 377-380.

[71] T. S. J. Lammerink, M. Elwenspoek, and J. H. J. Fluitman, "Thermal actuation of clamped silicon microbeams," *Sens. Materials*, vol. 3, pp. 217-238, 1992.

[72] C. Kuratli, and Q. Huang, "A fully-integrated self-calibrating transmitter/receiver IC for an ultrasound presence detector microsystem," in *Digest Tech. Papers IEEE ISSCC 1997*, San Francisco, 1997, pp. 196-197; and *J. Solid State Circuits*, in press.

[73] M. Hornung, O. Brand, O. Paul, H. Baltes, C. Kuratli, and Q. Huang, "Micromachined acoustic Fabry-Perot system for distance measurement," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 98*, Heidelberg, 1998, pp. 643-648.

[74] M. Hornung, R. Frey, O. Brand, H. Baltes, and C. Hafner, "Ultrasound barrier based on packaged micromachined membrane resonators," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems MEMS 95*, Amsterdam, 1995, pp. 334-339.

[75] R. Berger, C. Gerber, H.-P. Lang, and J. K. Gimzewski, "Micromechanics: a toolbox for femtoscale science: towards a laboratory on a tip," *Microelectronic Engineering*, vol. 35, pp. 373-379, 1997.

[76] A. Hierlemann, U. Weimar, G. Kraus, M. Schweizer-Berberich, and W. Göpel, "Polymer-based sensor arrays and multicomponent analysis for the detection of hazardous organic vapors in the environment," *Sens. Actuators B*, vol. 26-27, pp. 126-134, 1995.

[77] D. Lange, O. Brand, and H. Baltes, "CMOS chemical microsensors based on resonant cantilever beams," in *Proc. SPIE Symp. Smart Structures and Materials*, San Diego, CA, 1998, accepted.

[78] A. Nathan, and H. Baltes, *Microtransducer CAD*, Wien: Springer, 1998, in press.

[79] D. K. Schroder, *Semiconductor Material and Device Characterization*, New York: Wiley, 1990.

[80] H. Baltes, J. G. Korvink, and O. Paul, "Numerical modeling and material characterization for integrated micro electro mechanical systems", in *Simulation of Semiconductor Devices and Processes*, eds. H. Ryssel and P. Pichler, Wien: Springer, 1995, pp. 1-9.

[81] H. Baltes, O. Paul, and J. G. Korvink, "Simulation toolbox and material parameter data base for CMOS MEMS", in *Proc. 7th Intl. Symposium on Micro Machine and Human Science MHS'96*, Nagoya, 1996, pp. 1-8.

[82] O. Paul, M. von Arx, and H. Baltes, "Process-dependent thermophysical properties of CMOS IC thin films", in *Digest Tech. Papers Transducers*, vol. 1, Stockholm, 1995, pp. 528-531.

[83] M. von Arx, *Thermophysical Properties of CMOS IC thin films*, Ph.D. thesis, ETH Zurich, Switzerland, 1998, in preparation.

[84] F. Völklein, and H. Baltes, "A microstructure for measurement of thermal conductivity of polysilicon thin films", *J. Microelectromech. Syst.*, vol. 1, pp. 193-196, 1993.

[85] O. Paul, J. Korvink, and H. Baltes, "Determination of the thermal conductivity of CMOS IC polysilicon", *Sens. Actuators A*, vol. 41-42, pp. 161-164, 1994.

[86] M. B. Kleiner, S. A. Kühn, and W. Weber, "Thermal conductivity of thin silicon dioxide films in integrated circuits", in *Proc. 25th European Solid State Device Research Conference ESSDERC 1995*, pp. 473-476.

[87] T. H. Geballe, and G. W. Hull, "Seebeck effect in silicon", *Phys. Rev.*, vol. 98, no. 4, pp. 940-947, 1955.

[88] A. W. van Herwaarden, and P. M. Sarro, "Thermal sensors based on the Seebeck effect", *Sens. Actuators*, vol. 10, pp. 321-346, 1986.

[89] O. Paul, and H. Baltes, "Measuring thermogalvanomagnetic properties of polysilicon for the optimization of CMOS sensors", in *Digest Tech. Papers Transducers 93*, Yokohama, 1993, pp. 606-609.

[90] M. von Arx, O. Paul, and H. Baltes, "Test structures to measure the Seebeck coefficient of CMOS IC polysilicon", *IEEE Trans. Semiconductor Manufacturing*, vol. 10, no. 2, pp. 201-208, 1997.

[91] M. von Arx, O. Paul, and H. Baltes, "Determination of the heat capacity of CMOS layers for optimal CMOS sensor design", *Sens. Actuators A*, vol. 46-47, pp. 428-431, 1995.

[92] M. von Arx, O. Paul, and H. Baltes, "Test structures to measure the heat capacity of CMOS IC sandwiches", in *Proc. IEEE Intl. Conf. on Microelectronic Test Structures ICMTS'97*, Monterey, 1997, pp. 203-208.

[93] M. von Arx, O. Paul, and H. Baltes, "Thermoelectric test structure to measure the heat capacity of CMOS layer sandwiches", in *Digest Tech. Papers Transducers 97*, vol. 1, Chicago, 1997, pp. 619-622.

[94] D. Mahdevan, "Sensor packaging and assembly with a case study," *Canadian Workshop on Micro Electro Mechanical Systems*, University of Waterloo, Ontario, Canada, 1996, oral presentation.

[95] M. Waelti, N. Schneeberger, O. Paul, and H. Baltes, "Low temperature packaging of CMOS infrared microsystems by Si-Al-Au bonding," *Electrochem. Soc. Proc.*, vol. 97-36, pp. 147-154, 1998.